EE 330
Lecture 7

Propagation Delay

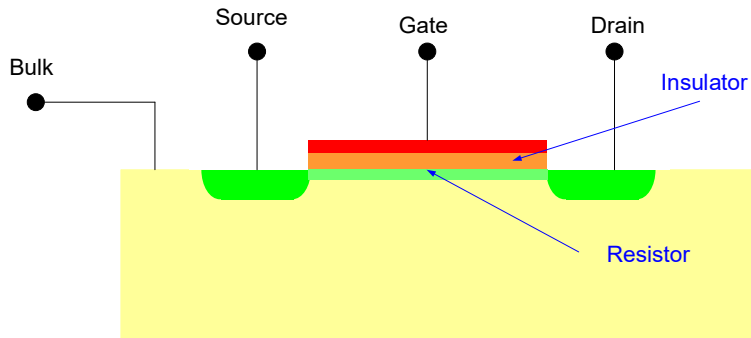# MOS Transistor

Qualitative Discussion of n-channel Operation

Source Gate Drain

Bulk
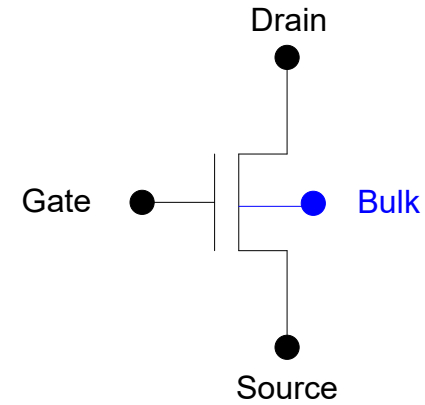
Insulator

n-channel MOSFET

For V_{GS} small

Source Gate Drain

Bulk

Insulator

Resistor

n-channel MOSFET

For V_{GS} large

Drain

Gate Bulk

Source
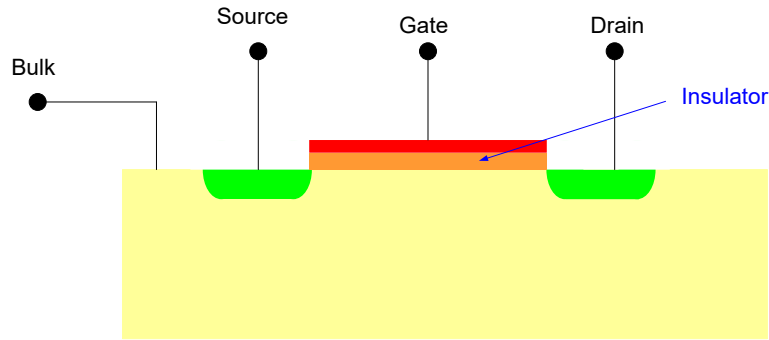
MOSFET actually 4-terminal device

- Region under gate termed the "channel"
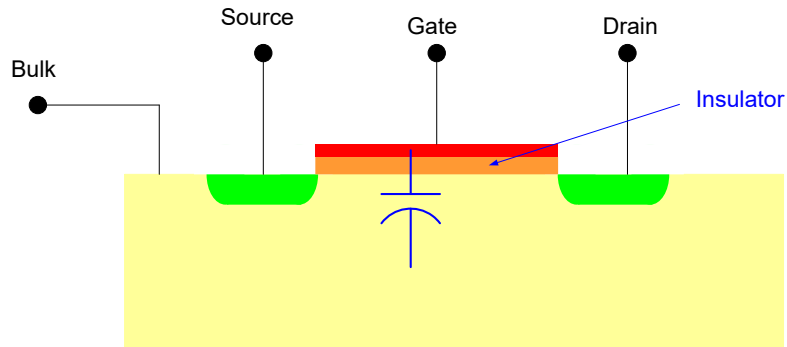- When "resistor" is electrically created, region where it resides in channel is termed an "inversion region"

MOS Transistor

Qualitative Discussion of n-channel Operation

Source   Gate   Drain

Bulk

Insulator

n-channel MOSFET

For V_{GS} small

Source   Gate   Drain

Bulk

Insulator

n-channel MOSFET

For V_{GS} large

Drain

Gate   Bulk

Source
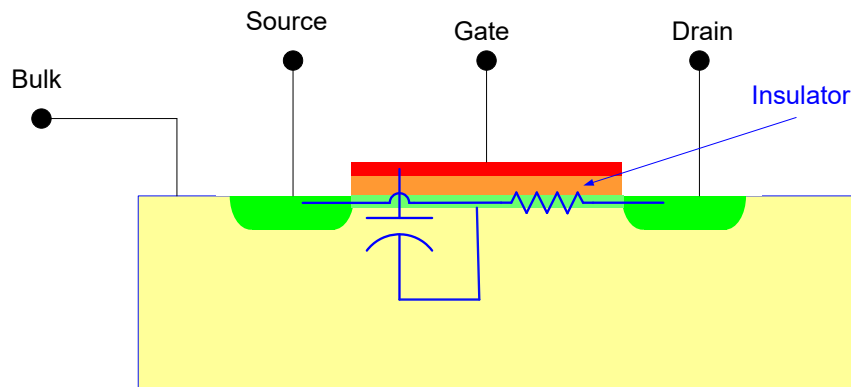
- Electrically created inversion layer forms a "thin "film" resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with
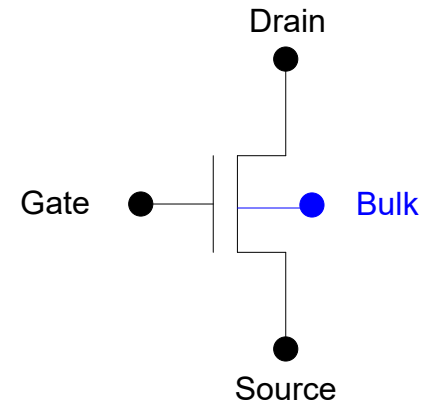
MOS Transistor

Qualitative Discussion of p-channel Operation
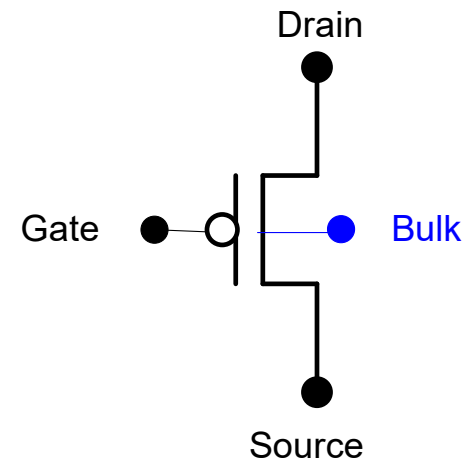
Source Gate Drain

Bulk

Insulator

p-channel MOSFET

For |V$_{GS}$| small

Source Gate Drain

Bulk

Insulator

p-channel MOSFET
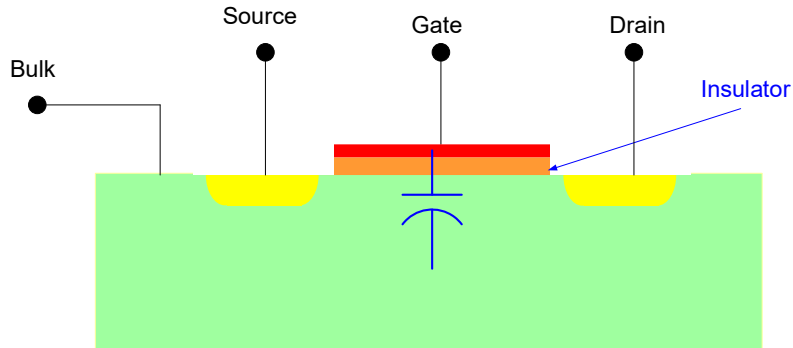
For |V$_{GS}$| large

Drain

Gate Bulk

Source

- Electrically created inversion layer forms a "thin "film" resistor
- Capacitance from gate to channel region is distributed
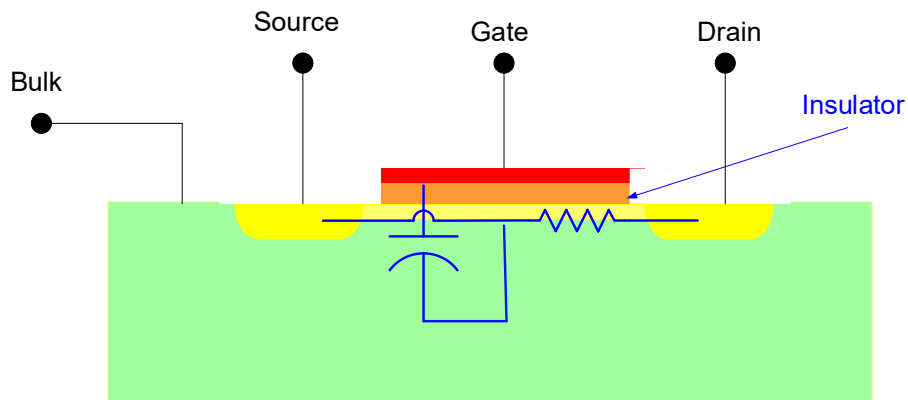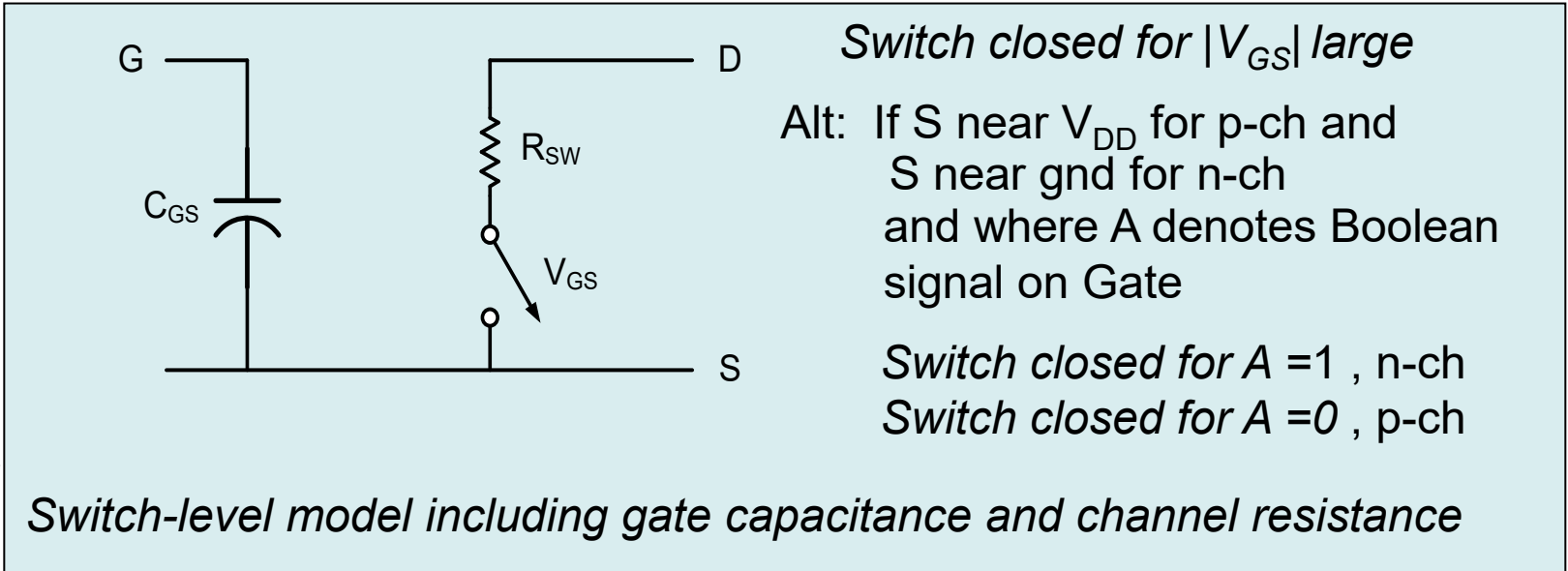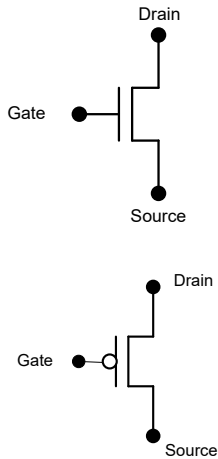- Lumped capacitance much easier to work with

Improved Switch-Level Model

Switch closed for $|V_{GS}|$ large

Alt: If S near V_{DD} for p-ch and
S near gnd for n-ch
and where A denotes Boolean
signal on Gate

Switch closed for A =1 , n-ch
Switch closed for A =0 , p-ch

Switch-level model including gate capacitance and channel resistance
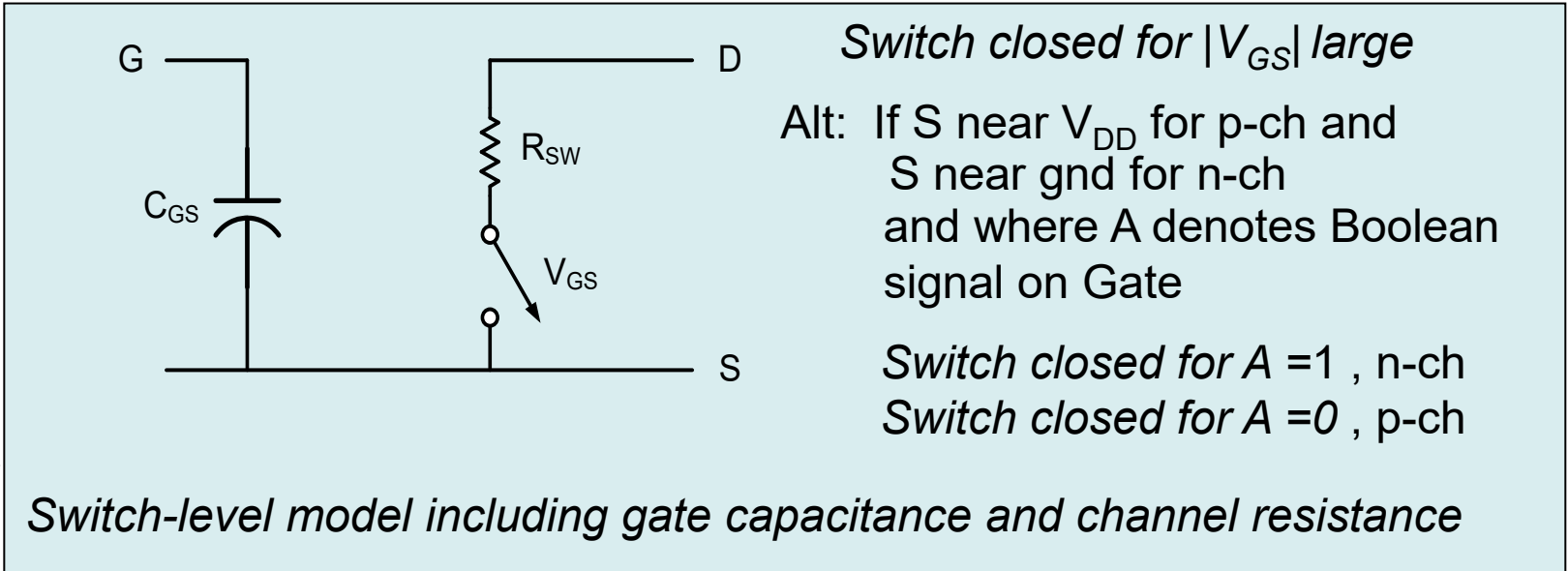
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process with V_{DD}=5V

$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \ \ n-channel \\ 6K\Omega \ \ p-channel \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Improved Switch-Level Model

Switch closed for $|V_{GS}|$ large

Alt: If S near V_{DD} for p-ch and
S near gnd for n-ch
and where A denotes Boolean
signal on Gate

Switch closed for A =1 , n-ch
Switch closed for A =0 , p-ch

Switch-level model including gate capacitance and channel resistance
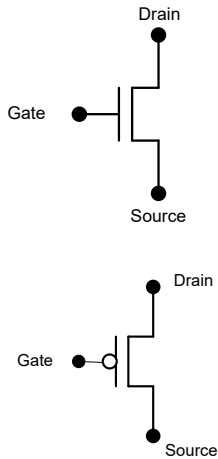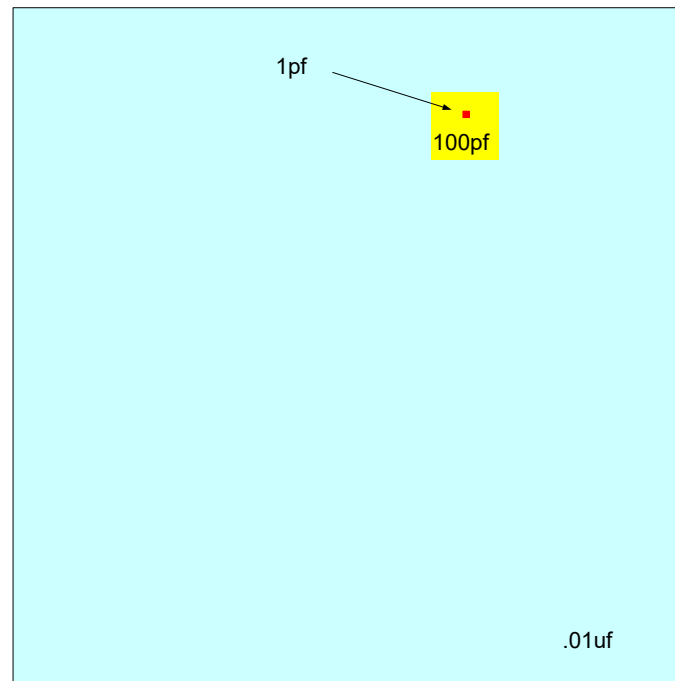
C_{GS} and R_{SW} dependent upon device sizes and process

Will assume for minimum-sized devices in a 0.18u process with V_{DD}=2V

$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Is a capacitor of 1.5fF small enough to be neglected?

1pf

100pf

.01uf

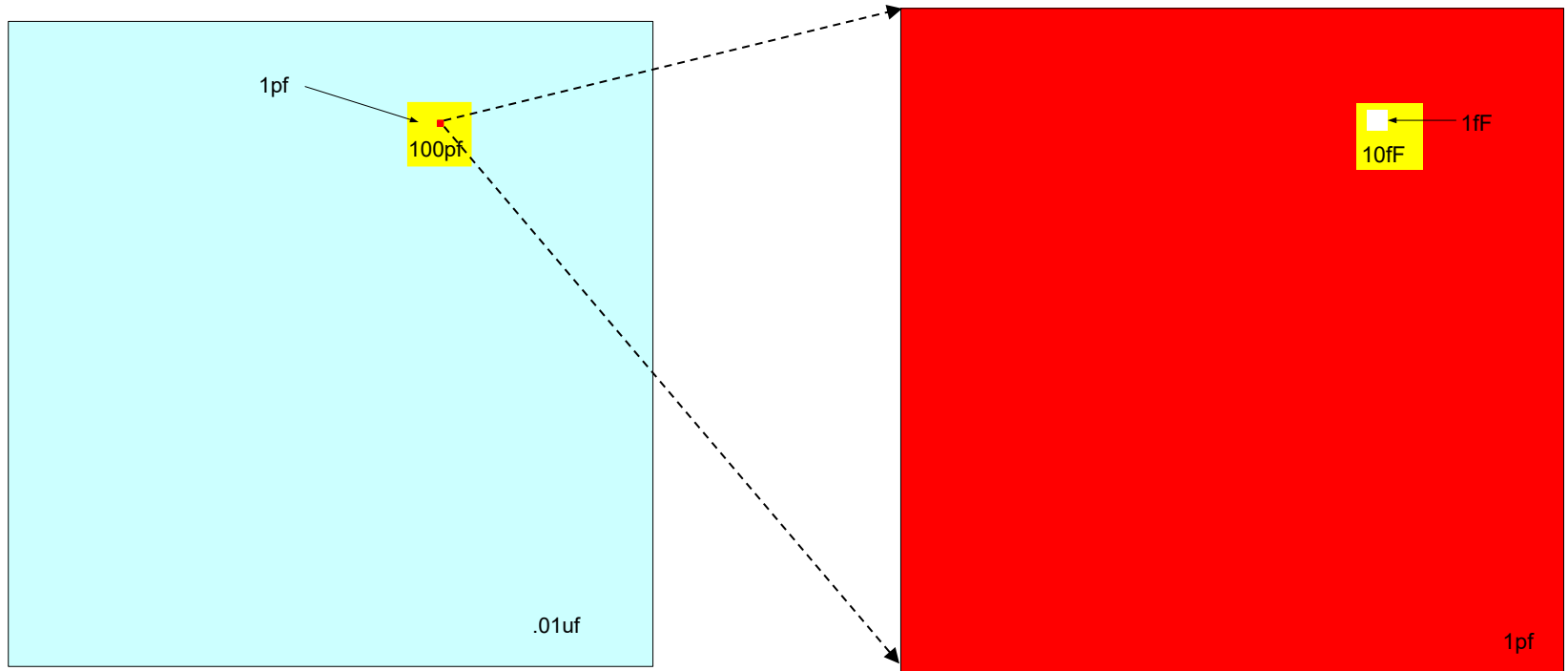**From EE 201 Parts Kit**

Capacitors (Farads)		
100p	3	
470p	3	
0.001u	3	2
0.0047u	3	2
0.01u	3	
0.047u	3	
0.1u	3	1
0.47u	3	
1u	3	
10u	3	
100u	3	

Area allocations shown to relative scale:

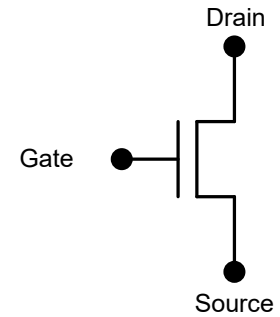# Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:

- **Not enough information at this point to determine whether this very small capacitance can be neglected**
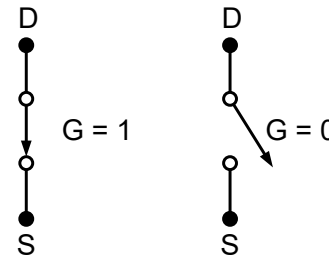- **Will answer this important question later**

Model Summary (for n-channel)
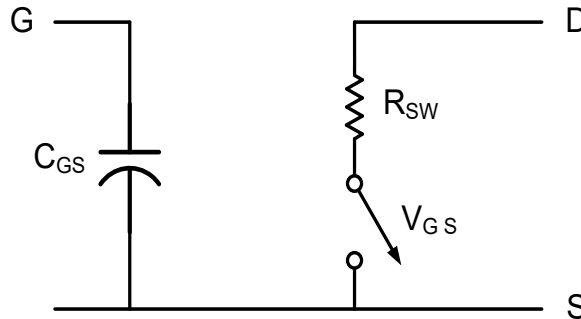
Drain

Gate

Source

1. Switch-Level model

D   D

$G = 1$ $G = 0$

S   S

2. Improved switch-level model

G   D

R_{SW}

C_{GS}

V_{GS}

S

Switch closed for V_{GS}= large

Switch open   for V_{GS}= small

Other models will be developed later

Model Summary (for p-channel)
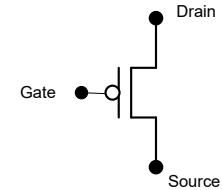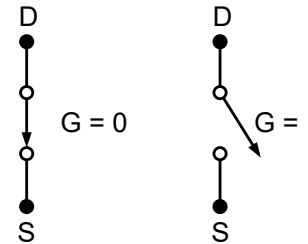
Gate ○— │ Drain
Source

1.   Switch-Level model

D   D
│   │
│ G = 0   │ G = 1
│   \
S   S

2.   Improved switch-level model

G ——————┐   ┌—————— D
        │   │
        │   ⌇ R$_{SW}$
    C$_{GS}$ ═╪═   │
        │   ○
        │   ↘ V$_{GS}$
        │   ○
        └————————┴—————— S
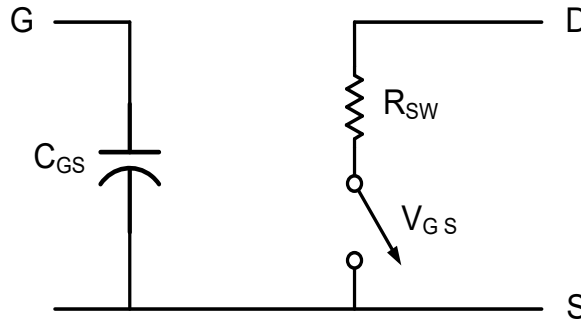
Switch closed for |V$_{GS}$|= large
Switch open   for |V$_{GS}$|= small
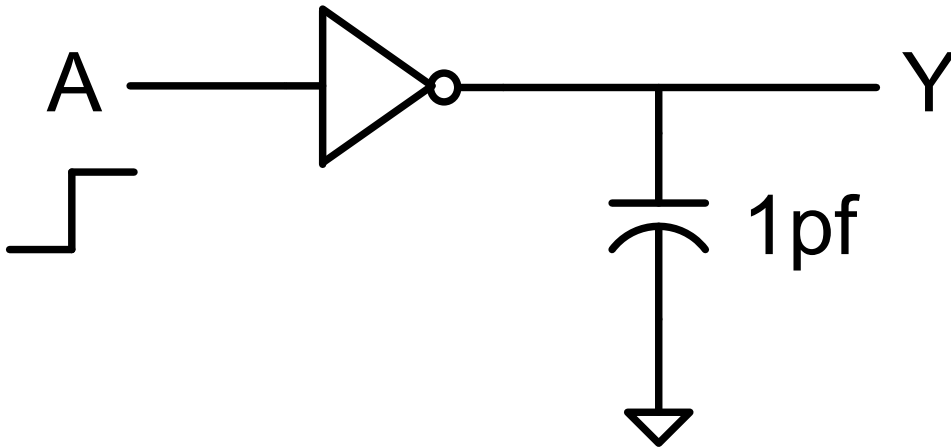
Other models will be developed later

Propagation Delay

Example

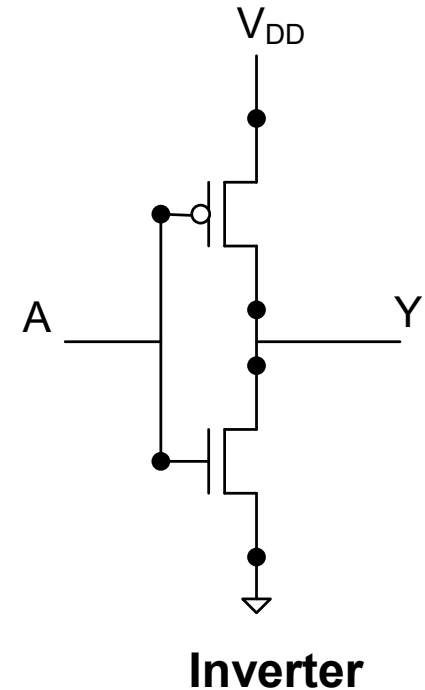## *What are t_{HL} and t_{LH}?*
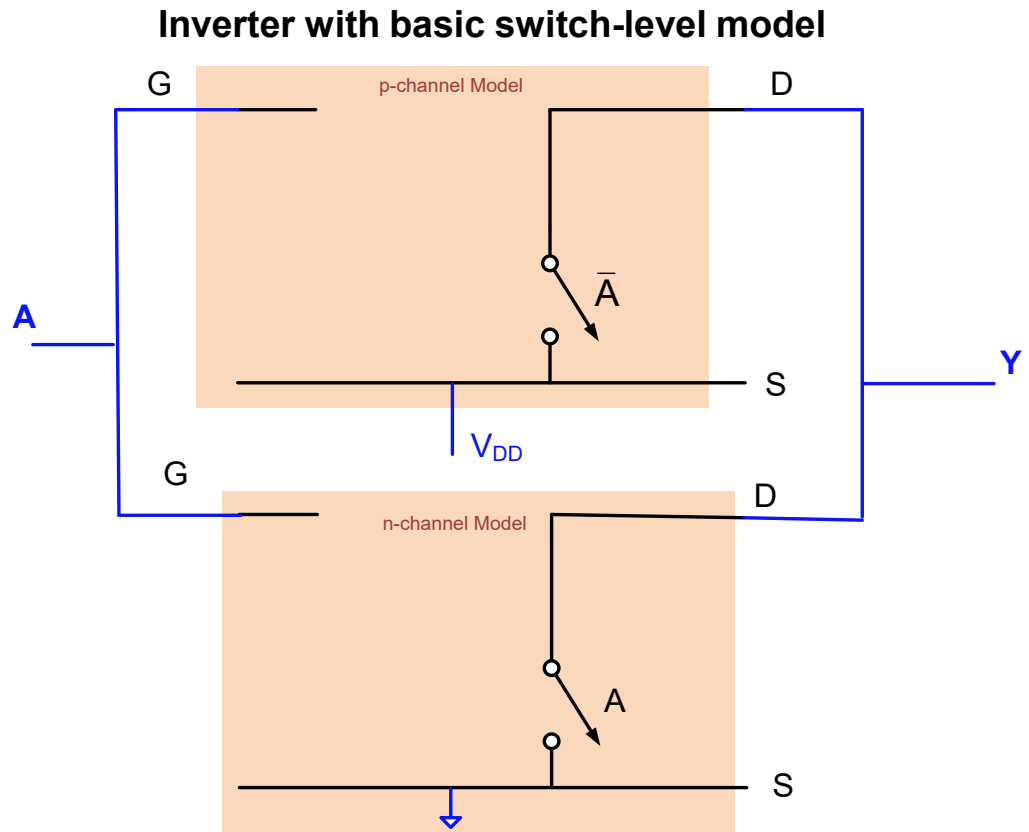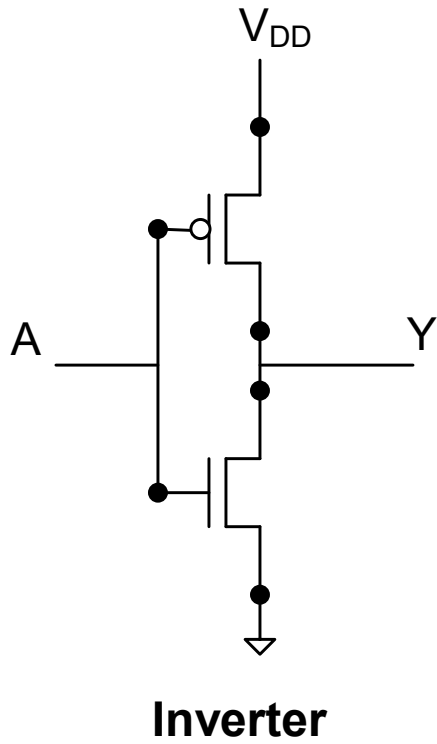
Assume $V_{DD}=5V$

Inverter

With basic switch level model ?

With improved switch level model ?

Example

Inverter

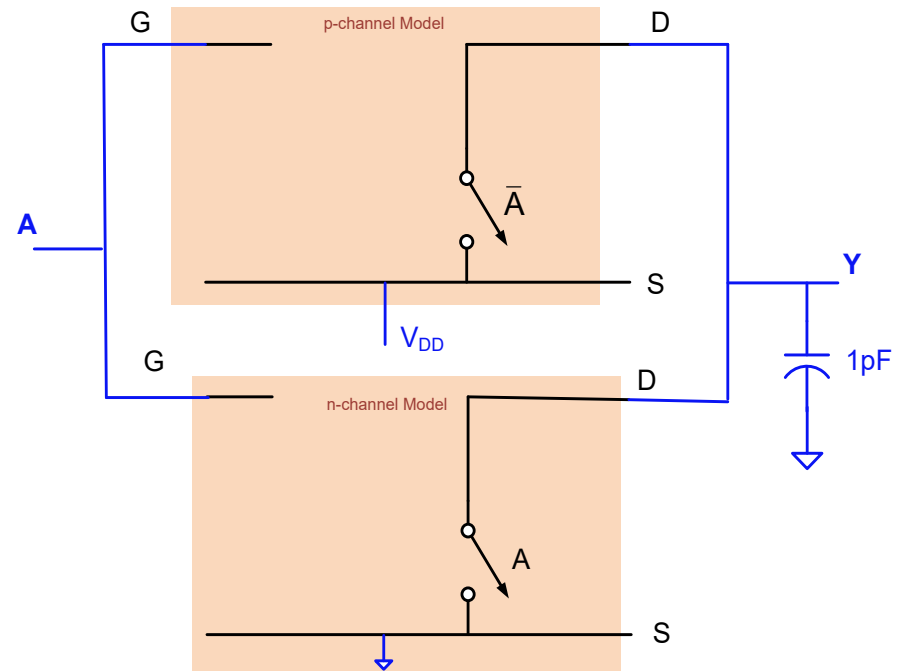**Inverter with basic switch-level model**

Example   *What are t_{HL} and t_{LH} at output?*

A —▷o— Y

1pf
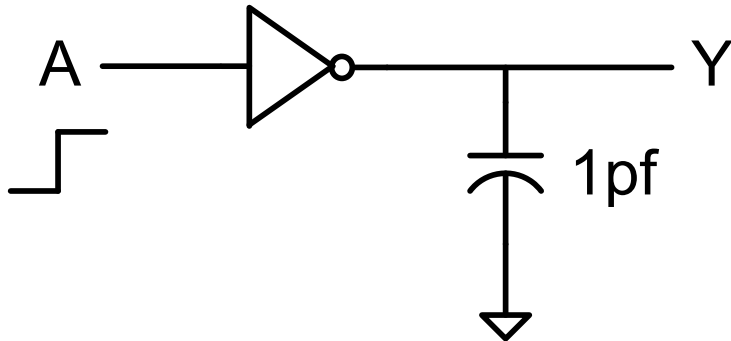
Assume ideal step at A input

With basic switch level model

A

Y

G   p-channel Model   D

$\bar{A}$

A

S

Y

V_{DD}

1pF

G   n-channel Model   D

A

S
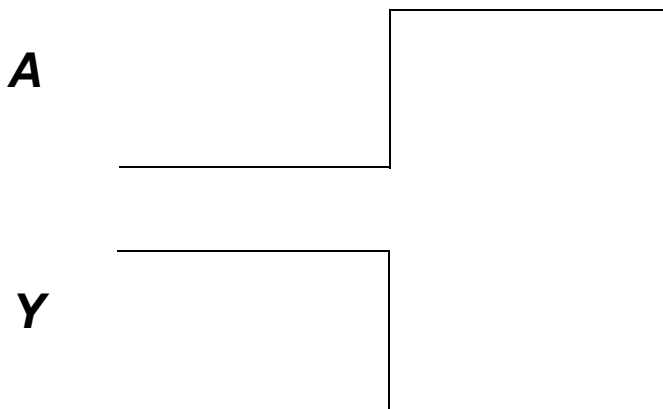
$t_{HL}=t_{LH}=0$

Example (cont)

With simple switch-level model $t_{HL}=t_{LH}=0$
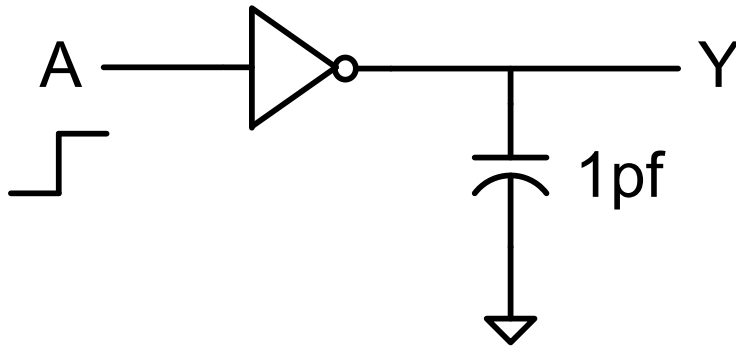
With improved model ?
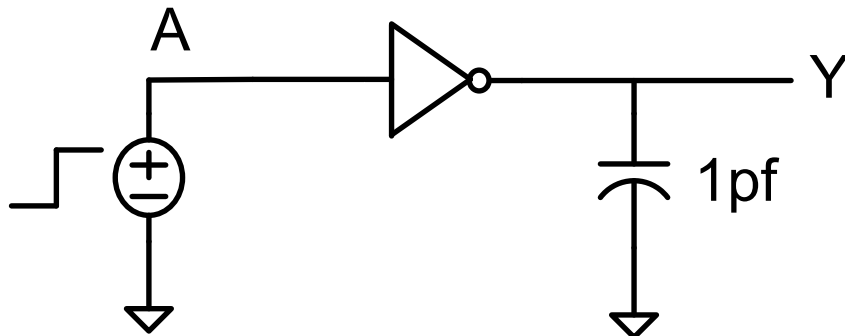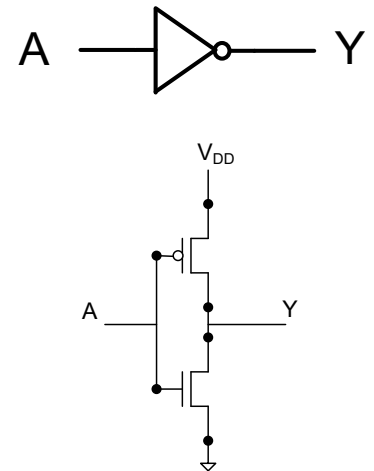
Inverter Model?

Example (cont)

Inverter with improved model

Inverter with Improved Model

Inverter Model
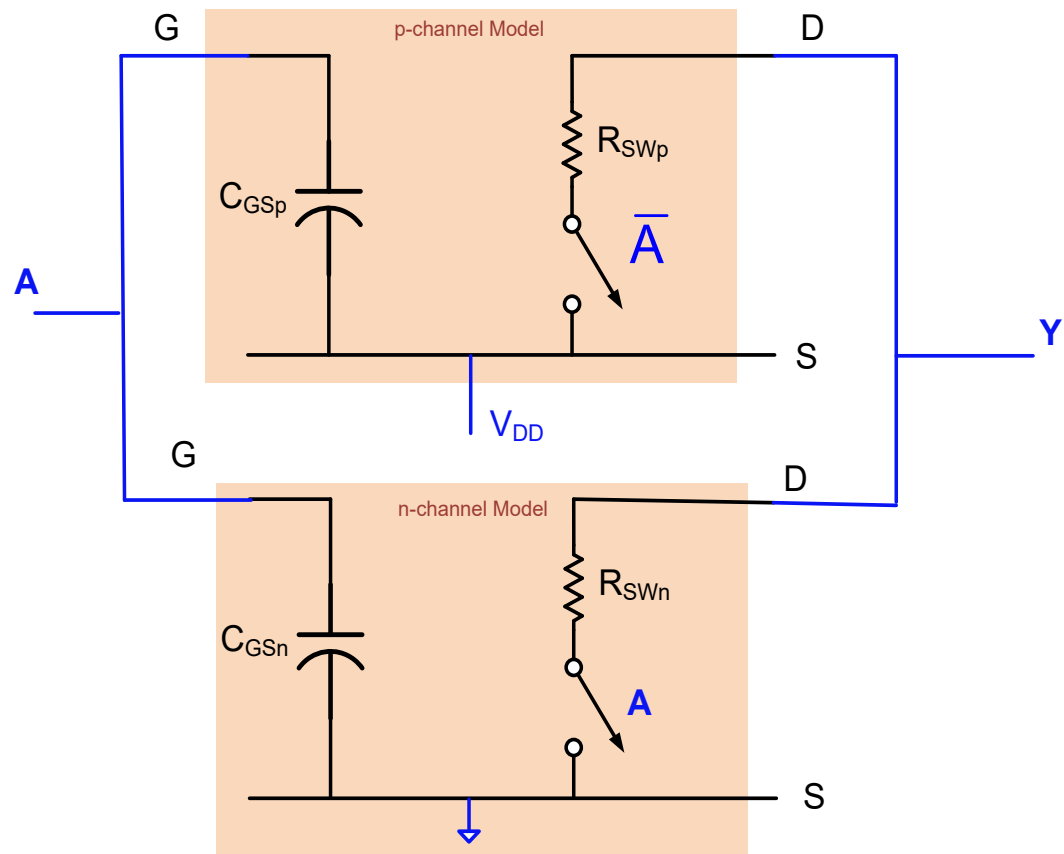
Example (cont)

With improved model $t_{HL}=?$
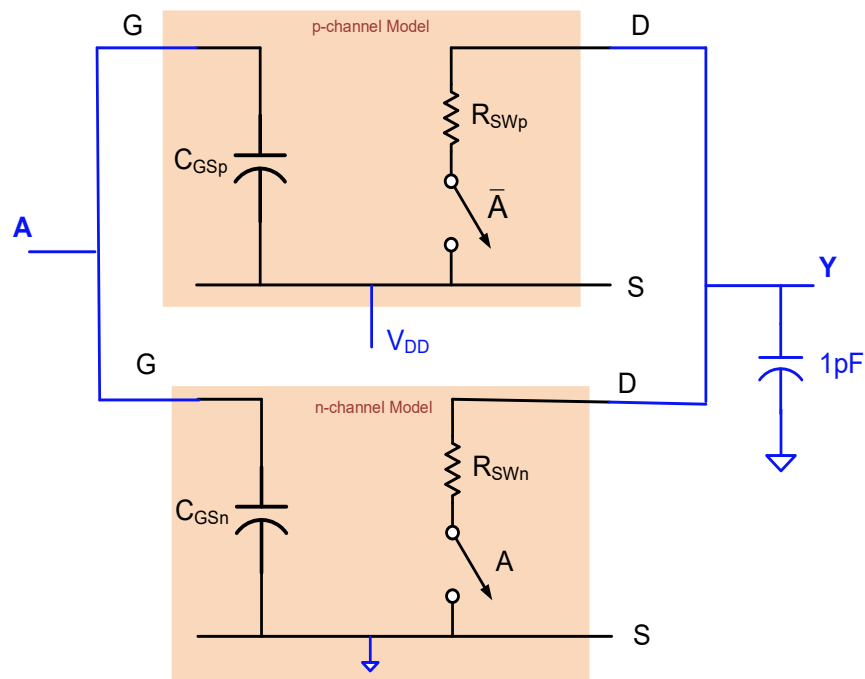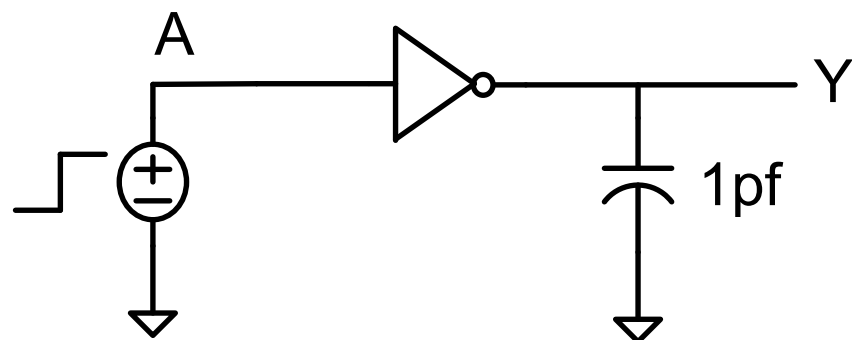
To initiate a HL output transition, assume Y has been in the high state for a long time, lower switch closes at time t=0, and upper switch opens just prior to t=0
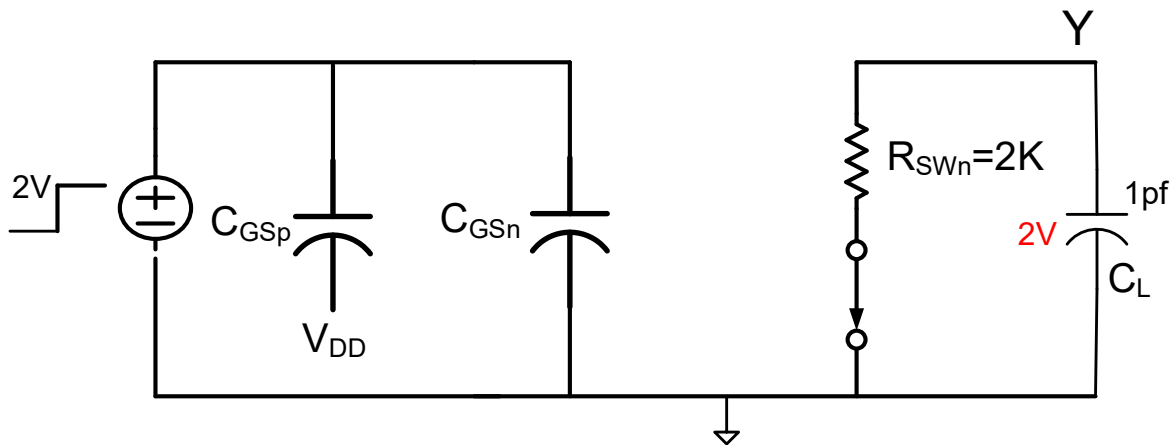
2V is the initial condition on C_L

Example (cont)

With improved model

$$t_{HL} = ?$$
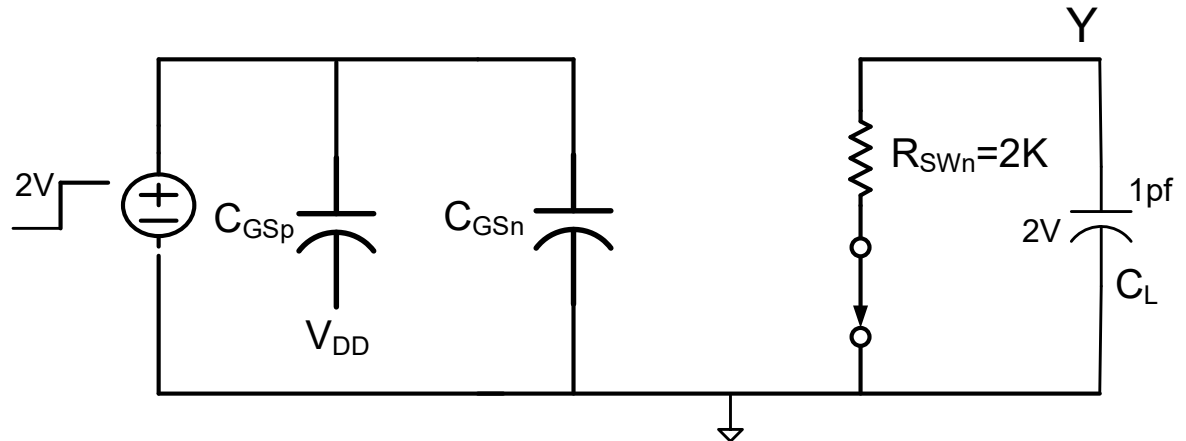
Recognize circuit (specifically on right) as a first-order RC network

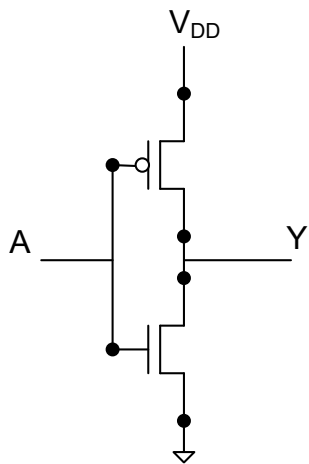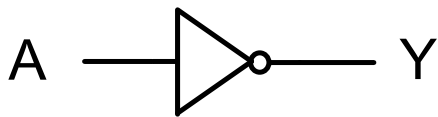**Recall: Step response of any first-order network with LHP pole can be written as**

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

where F is the final value, I is the initial value and τ is the time constant of the circuit

(from Chapter 7 of Nilsson and Riedel)

For the circuit above, F=0, I=2 and $\tau = R_{sWn} C_L$

Example (cont)

With improved model

$t_{HL}=?$

$Y=V_{OUT}$

$R_{SWn}=2K$

2V

C_{GSp} C_{GSn}

1pf

V_{DD}

C_L
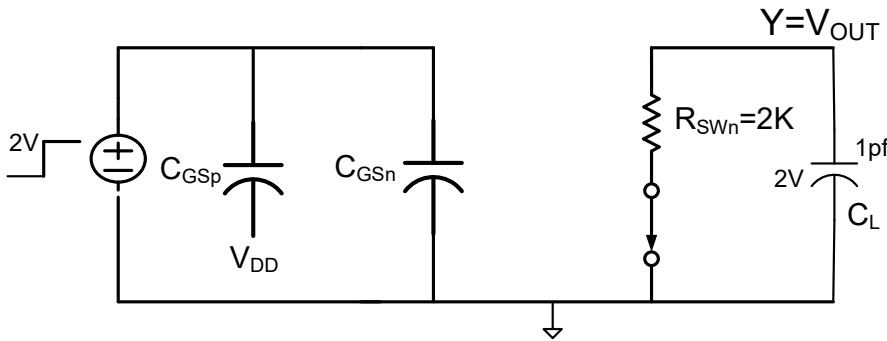
$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 2e^{-\frac{t}{\tau}}$$

$$\tau = R_{SWn}C_L$$

$I = 2V$

$F = 0V$

$t_{HL}=?$

$t_{HL}=?$

t
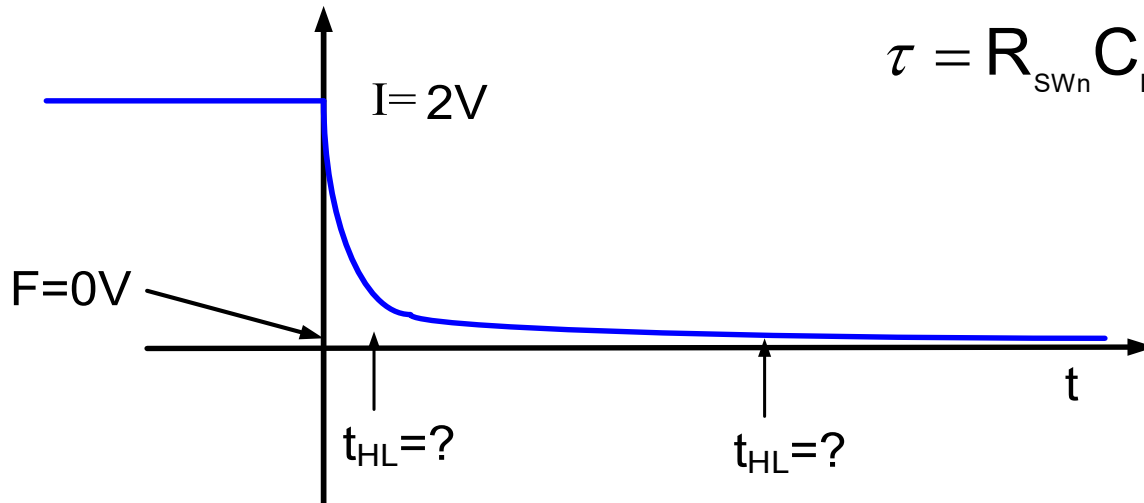
how is t_{HL} defined?

Example (cont)

$t_{HL}=?$

$I=2V, \quad F=0V$

$$\tau = R_{SWn}C_L$$

Define t_{HL} to be the time taken for output to drop to I/e

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \implies \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

Is this simply a mathematical definition or does it have some practical significance?

t_{HL} as defined here and as verified by experimental verification has proven useful at analytically predicting response time of circuits

Example (cont)

With improved model

$$\frac{I}{e} = F + (I - F) e^{-\frac{t_{HL}}{\tau}}$$

$$\frac{I}{e} = I e^{-\frac{t_{HL}}{\tau}}$$

$$\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}$$

$$t_{HL} = \tau$$

$I=2V, \quad F=0V$

$\tau = R_{SWn} C_L$

$$t_{HL} = R_{SWn} C_L$$
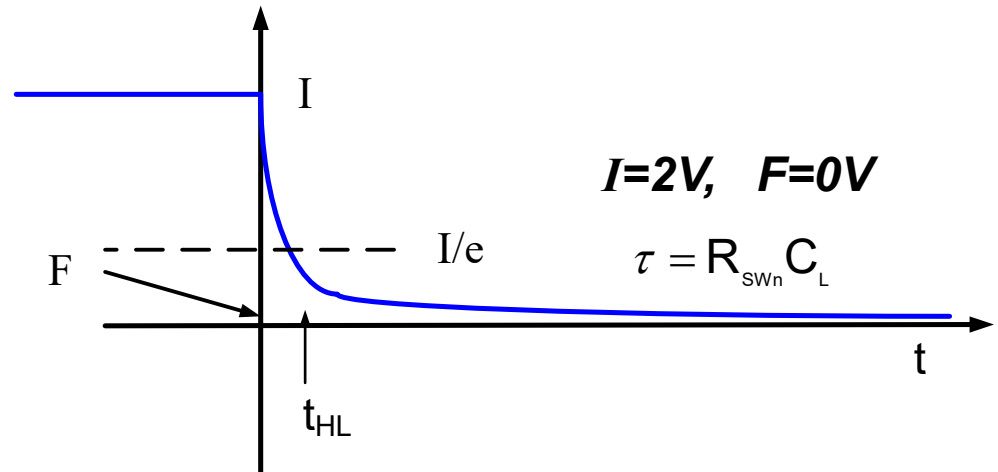
Both experimental results and accurate computer simulations show that this reasonably accurately predicts how quickly following stages recognize that a logic transition has taken place !!

Example (cont)

With improved model $t_{LH}=?$
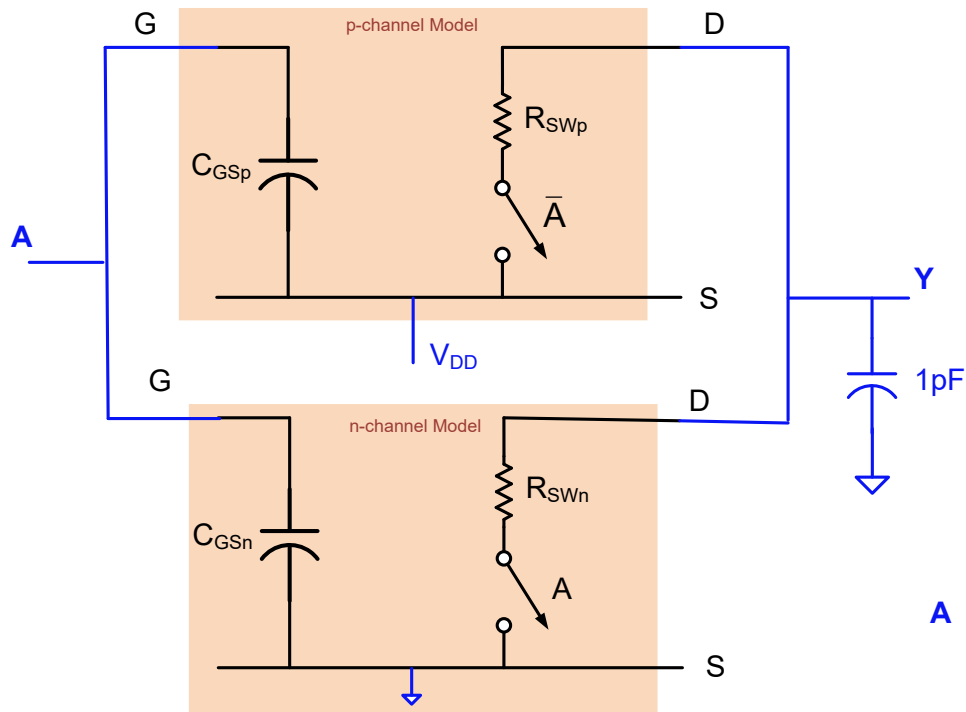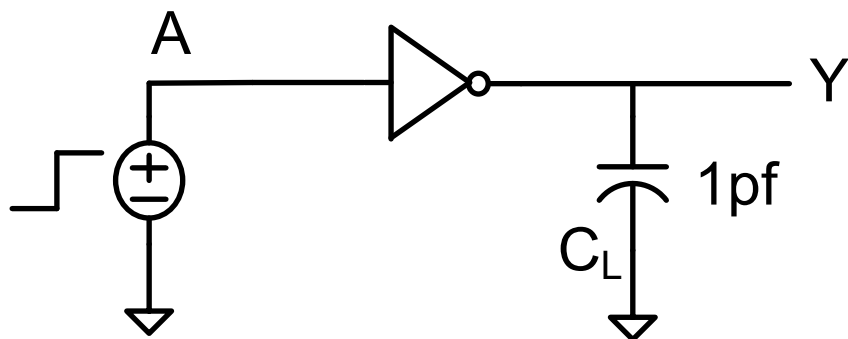
Assume output in low state for a long time and upper switch closes at time t=0 and lower switch opens just prior to t=0
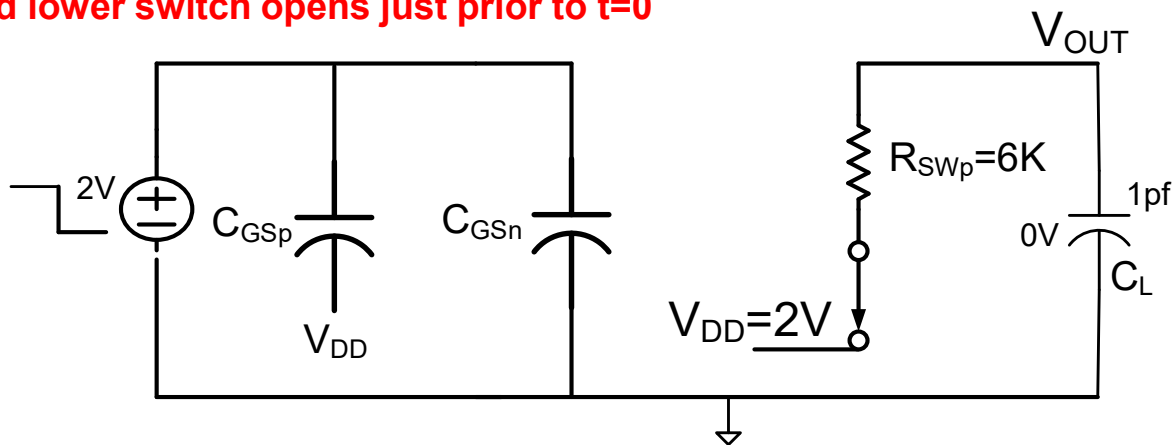
0V is the initial condition on C_L

Example (cont)

With improved model t_{LH}**=?**
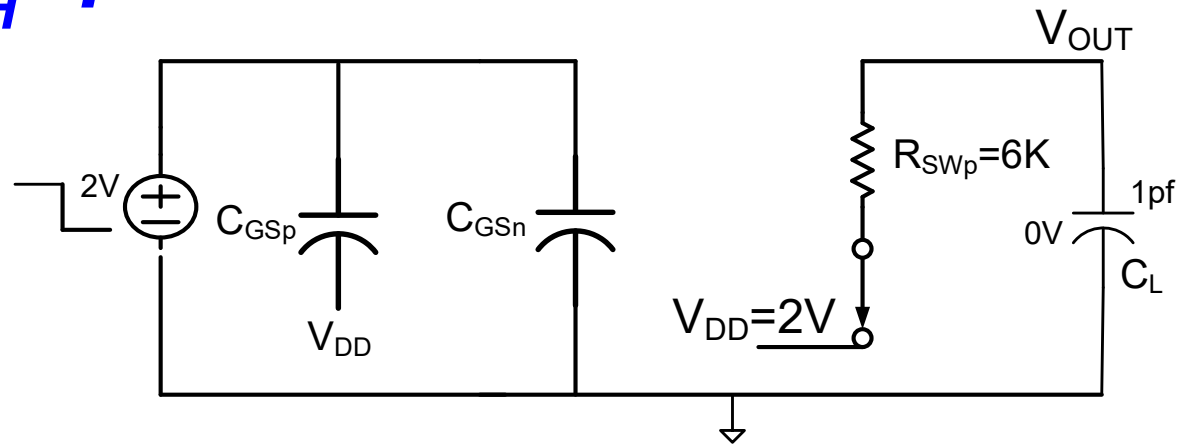
$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

For this circuit (specifically on the right), F=2, I=0 and $\tau = R_{SWp}C_L$

Example (cont)
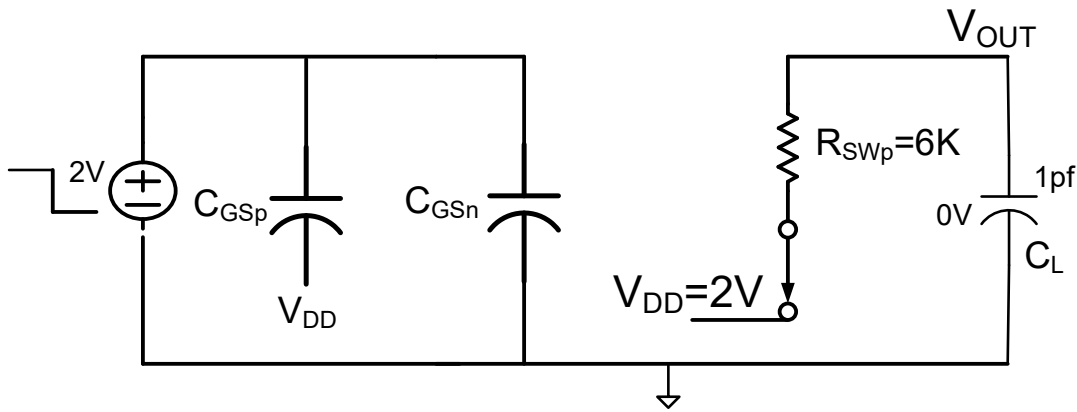
With improved model

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$
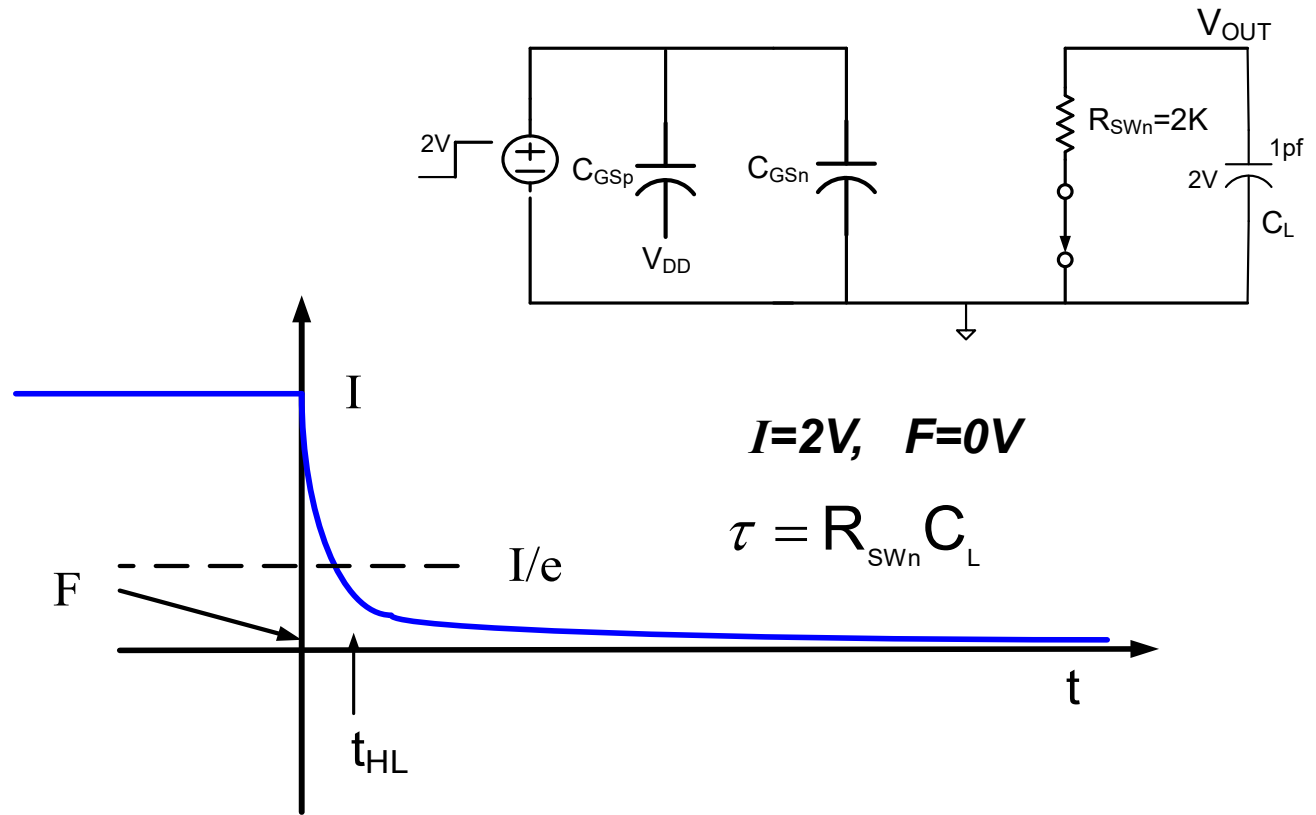
$$V_{OUT}(t) = 2\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\tau = R_{SWp}C_L$$

t_{LH}=?

R_{SWp}=6K

1pf

0V

C_L

V_{DD}=2V

V_{OUT}

2V

C_{GSp}

C_{GSn}

V_{DD}

F

I

t_{LH}=?

t_{LH}=?

t
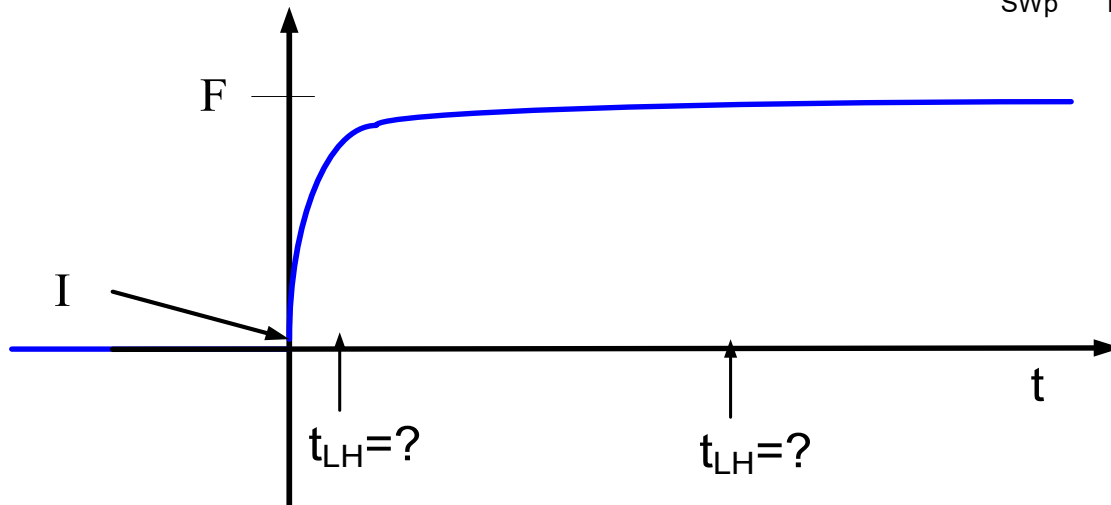
how is t_{LH} defined?

Example (cont)

With improved model

$t_{LH}=?$

Define t_{LH} as shown on figure

$I=0V, \quad F=2V$
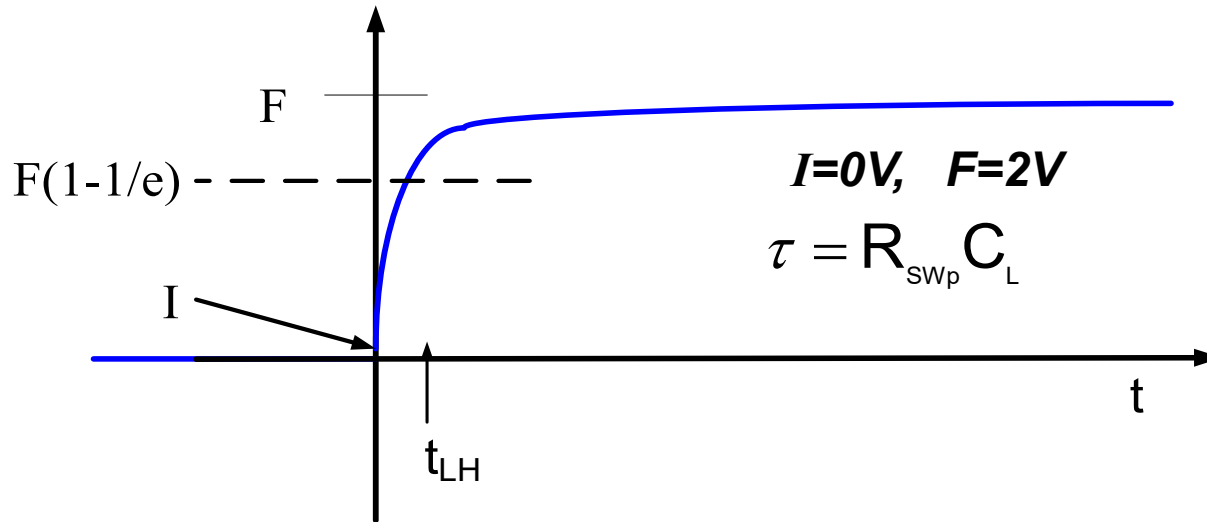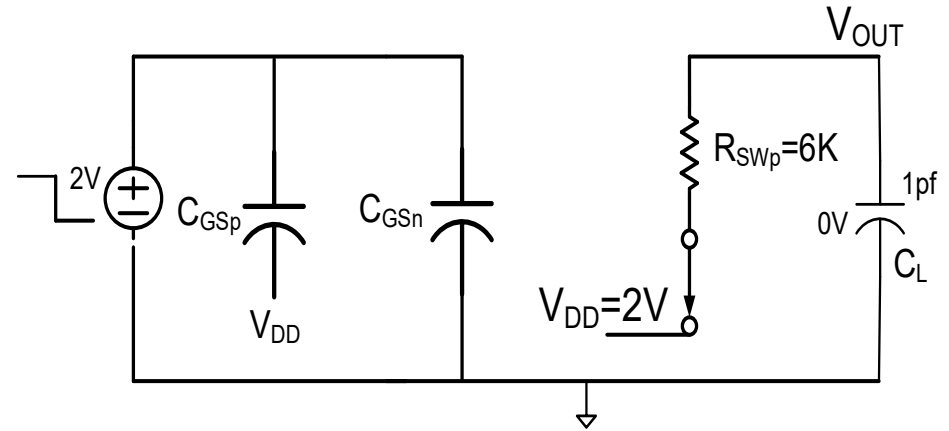
$$\tau = R_{SWp}C_L$$

t_{LH} as defined has proven useful for analytically predicting response time of circuits

$$V_{OUT}(t)=F+(I-F)e^{-\frac{t}{\tau}} \quad \Longrightarrow \quad F\left(1-\frac{1}{e}\right)=F+(I-F)e^{-\frac{t_{LH}}{\tau}}$$

Example (cont)

With improved model

$t_{LH}=?$

$$I=0V, \quad F=2V$$
$$\tau = R_{SWp}C_L$$

$$F\left(1-\frac{1}{e}\right)=F+(I-F)e^{-\frac{t_{LH}}{\tau}}$$

$$F\left(1-\frac{1}{e}\right)=F+(F)e^{-\frac{t_{LH}}{\tau}}$$

$$1-\frac{1}{e}=1+e^{-\frac{t_{LH}}{\tau}}$$

$$t_{LH}=\tau \qquad \Longrightarrow \qquad t_{LH}=R_{SWp}C_L$$

Example (cont)

With improved model

V_{OUT}

R_{SW}

C_{GSp} C_{GSn}

V_{DD}

1pf

C_L

2V

V_{OUT}

$R_{SWp}=6K$

C_{GSp} C_{GSn}

V_{DD}

$V_{DD}=2V$

0V

1pf

C_L

2V
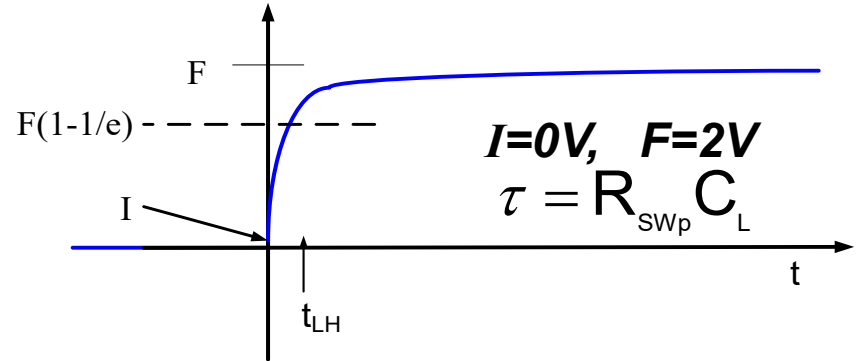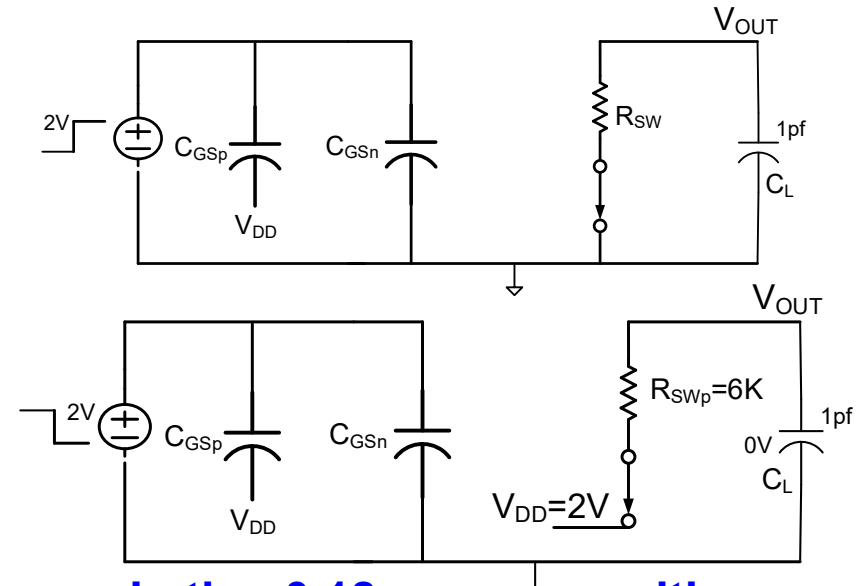
In the 0.18u process with minimum-sized devices

$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 1pF = 2n\sec$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 1pF = 6n\sec$$

Note this circuit is quite fast !

Note that t_{HL} is much shorter than t_{LH}

Often C_L will be even smaller and the circuit will be much faster !!

Summary: What is the delay of a minimum-sized inverter driving a 1pF load?

X

Y

C_L 1pF
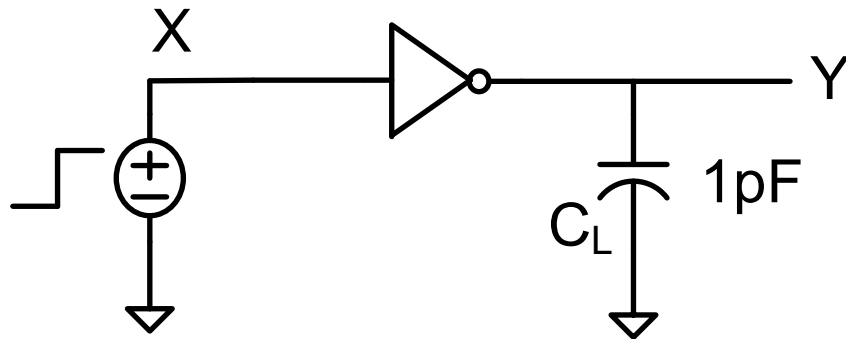
In a 0.18μ process

$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 1pF = 2n \sec$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 1pF = 6n \sec$$

Improved switch-level model
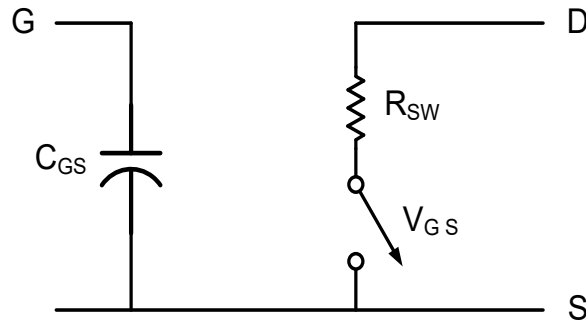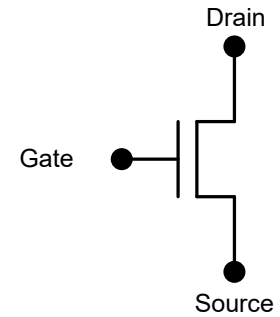
Switch closed for V_{GS}= large

Switch open   for V_{GS}= small

- **Previous example showed why R_{SW} in the model was important**

- **But of what use is the C_{GS} which did not enter the previous calculations?**

For minimum-sized devices in a 0.18µ process

$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \left. \begin{array}{l} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{array} \right\}$$

One gate often drives one or more other gates !
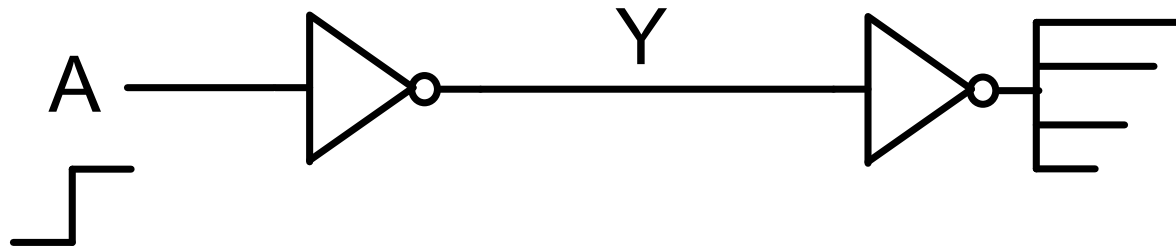
What are t_{HL} and t_{LH}?
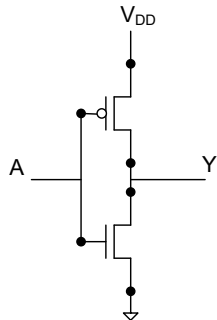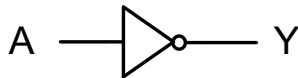
Example: What is the delay of a minimum-sized inverter driving another identical device?

?
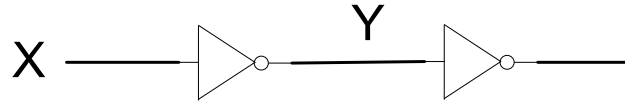
Load on first inverter

C_{GSn} and C_{GSp} both 1.5fF

$$C_{GSn} \cong C_{GSp} \cong 1.5\text{fF}$$
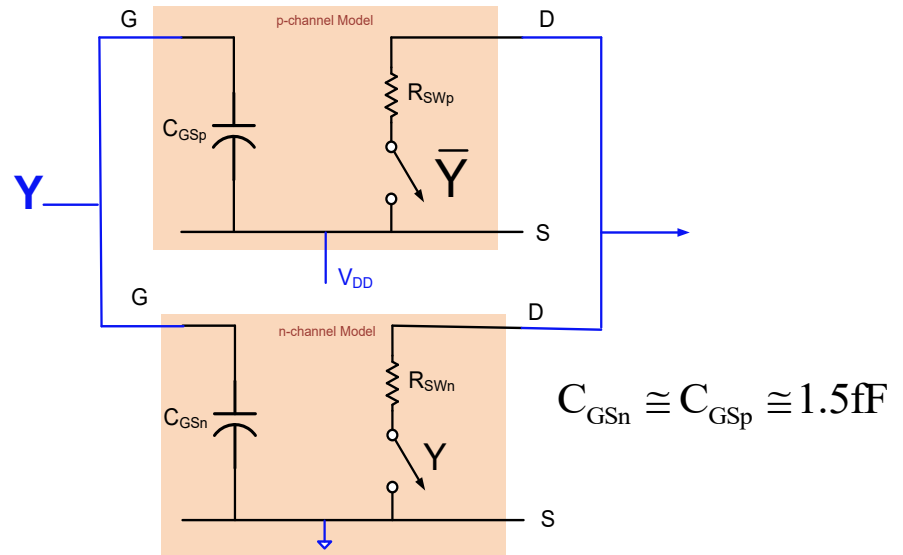
Loading effects same whether C_{GSp} and/or C_{GSn} connected to V_{DD} or GND

$C_{GSp}+C_{GSn}$

3fF
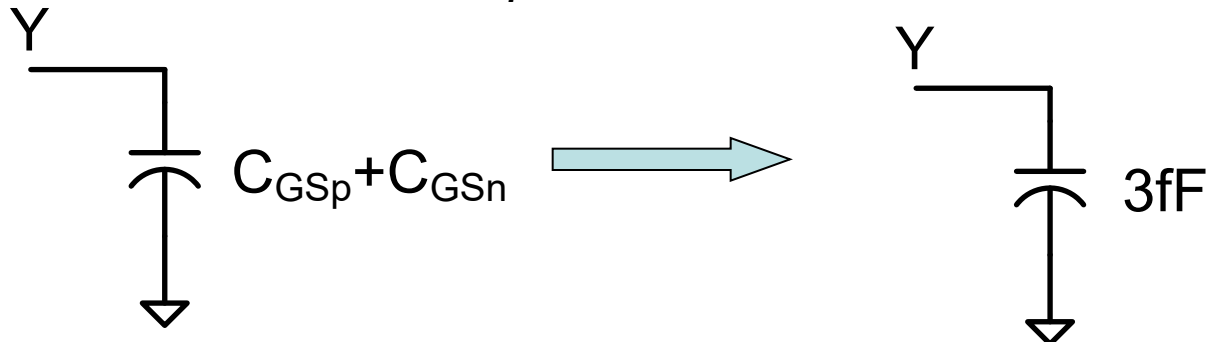
For convenience, will reference both to ground

Is a capacitor of 1.5fF small enough to be neglected?
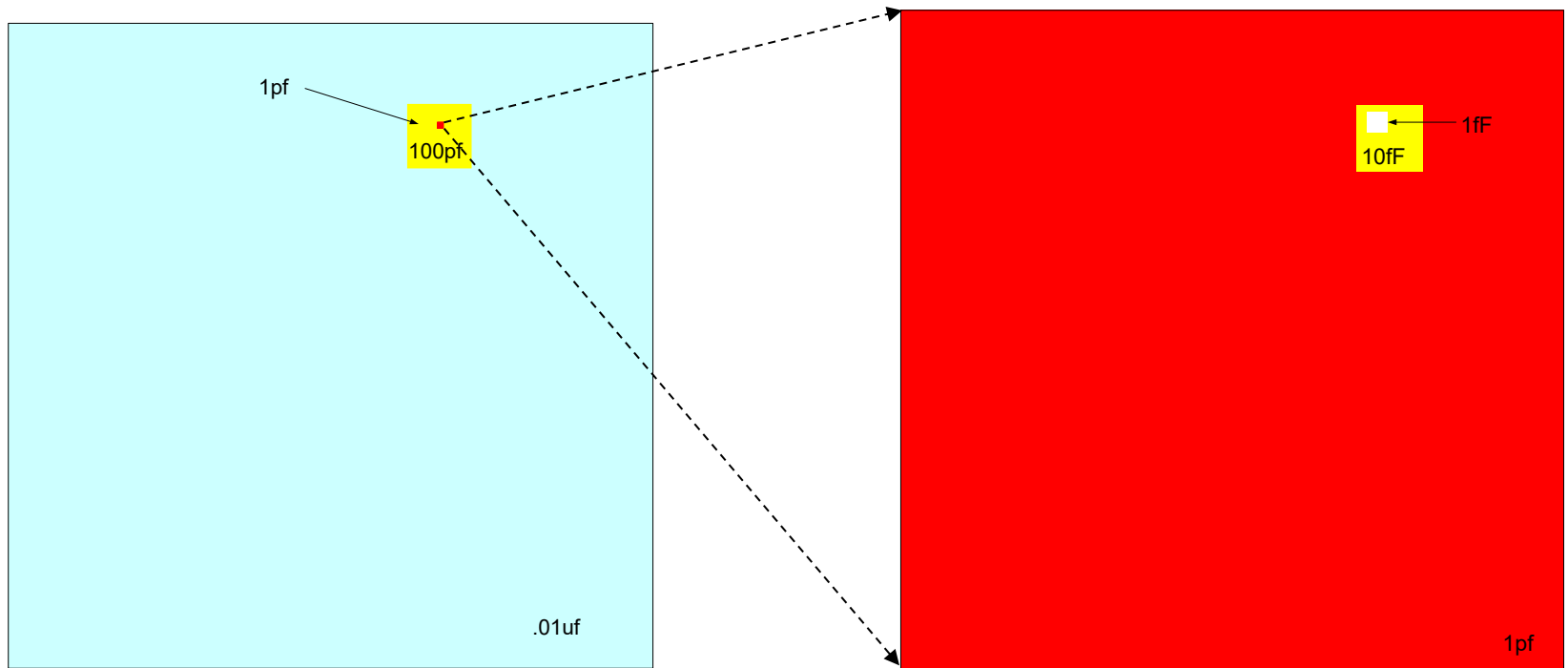
Area allocations shown to relative scale:

- **This example will provide insight into the answer of the question**

Example: What is the delay of a minimum-sized inverter driving another identical device? Assume $V_{DD}=2V$

X —————▷○———— Y ————▷○————

X ———————▷○——————— Y

⎓ (±)

⊥ 3fF
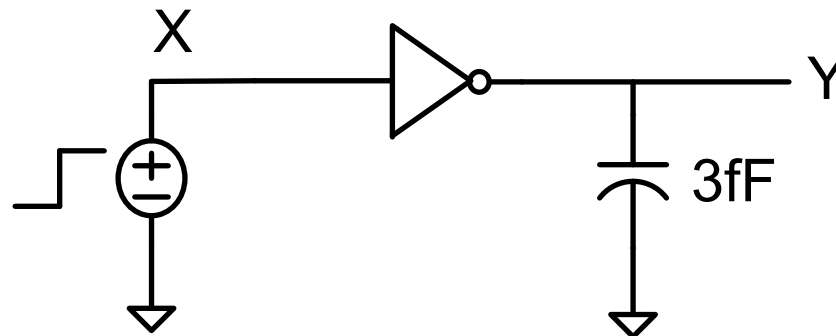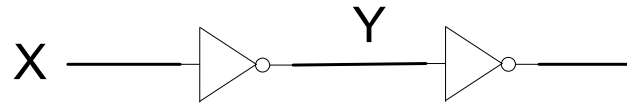
Generalizing the Previous Analysis to Arbitrary Load
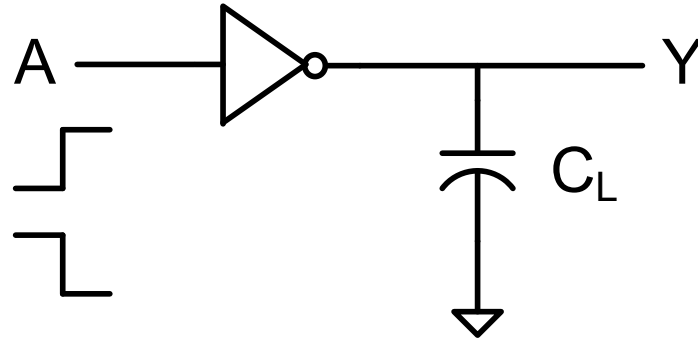
$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

Example: What is the delay of a minimum-sized inverter driving another identical device?
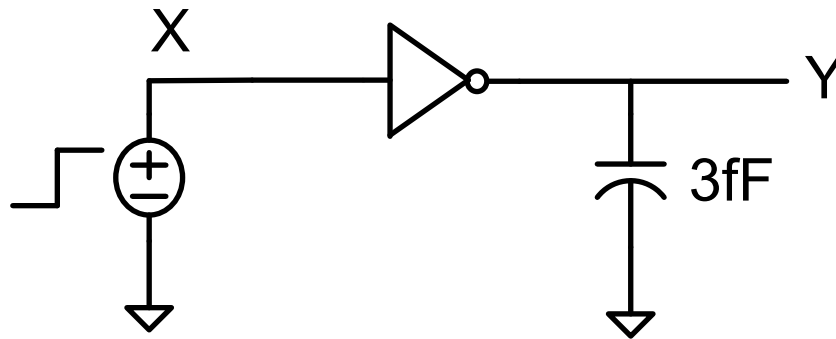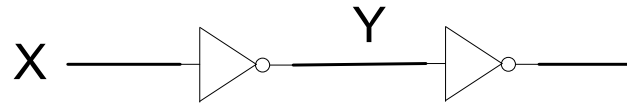
$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 3fF = 6p\sec$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 3fF = 18p\sec$$

Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?

Example: What is the delay of a minimum-sized inverter driving another identical device?
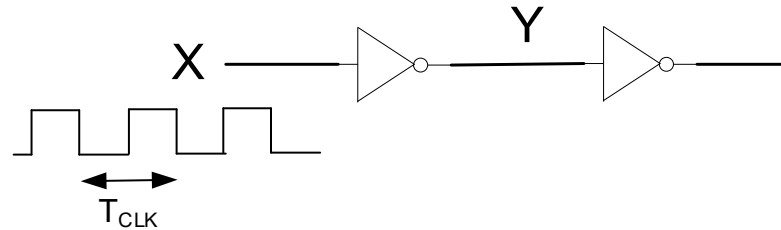
$$t_{HL} \cong R_{SWn} C_L = 6p\sec$$

$$t_{LH} \cong R_{SWp} C_L = 18p\sec$$

What would be the maximum clock rate for acceptable operation?

$$T_{CLK-min} = t_{HL} + t_{LH}$$

$$f_{CLK-max} = \frac{1}{T_{CLK-min}} = \frac{1}{24psec} = 40GHz$$

And much faster in a finer feature process !!   ??????

What would be the implications of allowing for 10 levels of logic and 10 loads (FanOut=10)?

Example: What is the delay of a minimum-sized inverter driving another identical device? SUMMARY
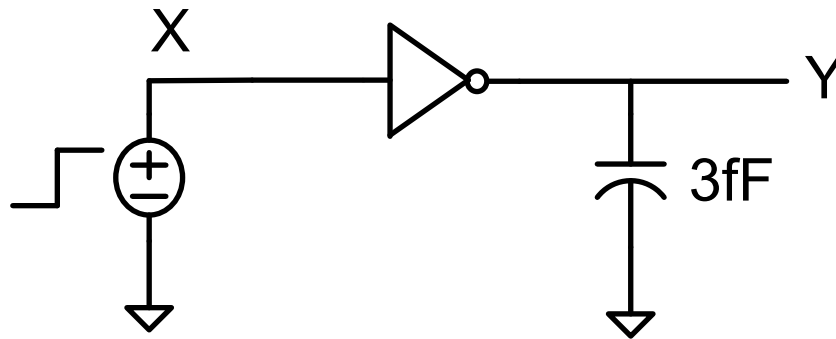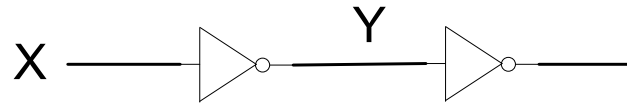
$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 3fF = 6p\sec$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 3fF = 18p\sec$$

This is very fast but even the small 1.5fF capacitors are not negligible !

These capacitors play a key role in determining the speed of a circuit !

Response time of logic gates
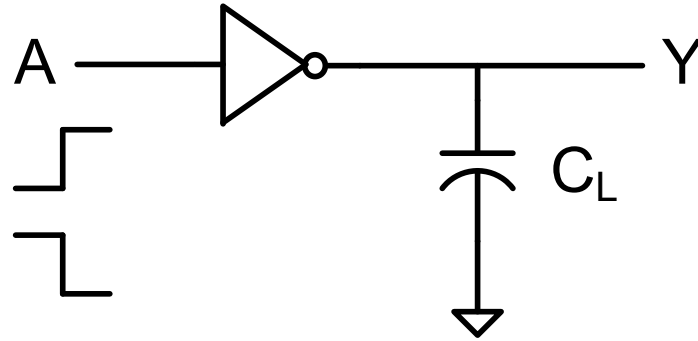
$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

- **Logic Circuits can operate very fast**
- **Extremely small parasitic capacitances play key role in speed of a circuit**

Some Observations about Technology and Politics

Are the larger feature size technologies still used by industry today in the US or abroad?

GlobalData predicts that the <u>Chinese market will play a much smaller role for foreign suppliers by 2030</u>. More than 90% of the chips sold and used worldwide involve low-process production technology.

https://www.investmentmonitor.ai/analysis/china-lead-global-semiconductor-growth 2030#:~:text=Global %20semiconductor%20industry%20revolves%20around,Samsung 20Electronics%20and%20SK%20Hynix.

China has been the biggest buyer of chipmaking gear for two straight years

■ China ■ Korea ■ Taiwan ■ Japan ■ North America ■ Europe ■ Rest of the World

2020	
■	$18.7B
■	$16.1B
■	$17.1B
■	$7.6B
■	$6.5B
■	$2.6B
■	$2.5B

Region

Source: SEMI

Some Observations about Technology and Politics

Sept 2022

https://technode.com/2021/03/04/where-china-is-investing-in-semiconductors-in-charts/

China is the world's largest consumer of semiconductors, and the lion's share of revenue from purchasing these chips go to foreign firms. China consumed $143.4 billion worth of wafers in 2020, and just 5.9% of them were produced by companies headquartered in China.

The Chips Act of 2022

$52 billion grant over five years to help grow the domestic semiconductor manufacturing. $2 billion of which is to explicitly focus on legacy chip production. These chips are essential to the auto industry, the military, and other industries critical to our national security interests.

By the numbers: The CHIPS Act directs $280 billion in spending over the next ten years. The majority—$200 billion—is for scientific R&D and commercialization. Some $52.7 billion is for semiconductor manufacturing, R&D, and workforce 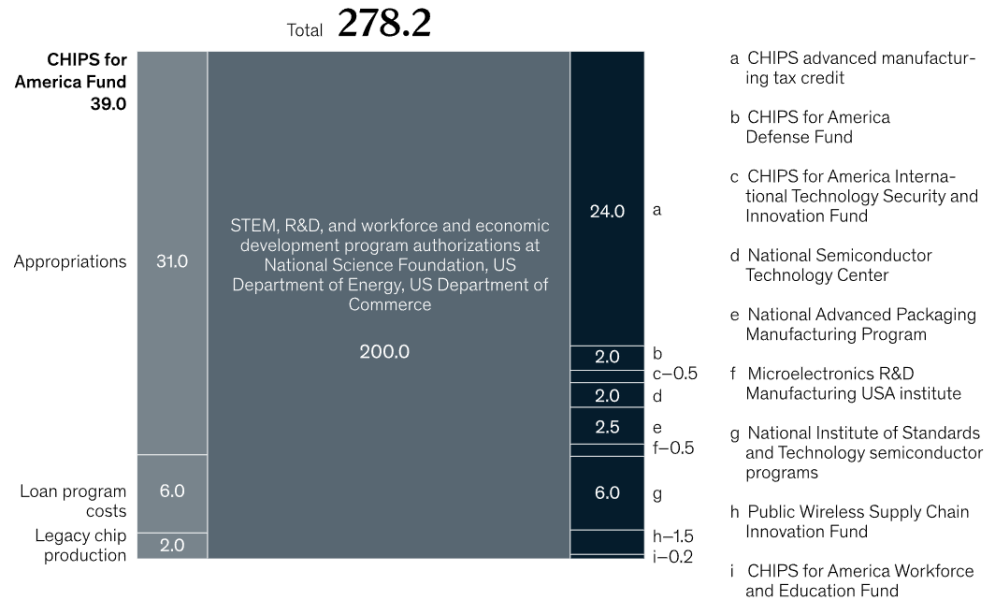development, with another $24 billion worth of tax credits for chip production. There is $3 billion slated for programs aimed at leading-edge technology and wireless supply chains.

The CHIPS and Science Act of 2022 directs $280 billion in spending over the next ten years, with the bulk for scientific R&D.

CHIPS and Science Act funding for 2022–26, $ billion

Total **278.2**

CHIPS for America Fund 39.0	
Appropriations 31.0	STEM, R&D, and workforce and economic development program authorizations at National Science Foundation, US Department of Energy, US Department of Commerce
	200.0
Loan program costs 6.0	
Legacy chip production 2.0	

24.0 a
2.0 b
c−0.5
2.0 d
2.5 e
f−0.5
6.0 g
h−1.5
i−0.2

a CHIPS advanced manufacturing tax credit

b CHIPS for America Defense Fund

c CHIPS for America International Technology Security and Innovation Fund

d National Semiconductor Technology Center

e National Advanced Packaging Manufacturing Program

f Microelectronics R&D Manufacturing USA institute

g National Institute of Standards and Technology semiconductor programs

h Public Wireless Supply Chain Innovation Fund

i CHIPS for America Workforce and Education Fund

Source: Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act of 2022, H.R. 4346, 117th Cong. (2022)

McKinsey & Company

How do I get CHIPS Act Funding?

<u>Breaking News</u>: The application for wafer manufacturers and suppliers of materials and equipment (e.g., chemicals and tools) was just released. Read the details <u>here</u>.

$53 billion is available for semiconductor manufacturing and R&D, plus a 25% refundable tax credit for qualified CapEx. See below to discover where your business fits in

Need help? Book an appointment with our professional grant writing team <u>here</u> or email us: equity@chipsact.com
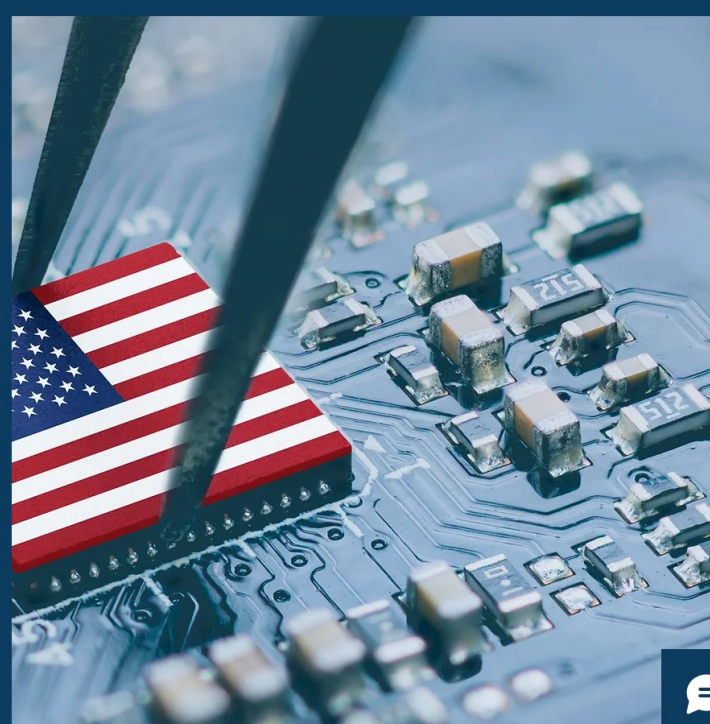
STATE OF THE U.S. SEMICONDUCTOR INDUSTRY

SEMICONDUCTOR INDUSTRY ASSOCIATION

2023

Stay Safe and Stay Healthy !

End of Lecture 7